**Digital Circuits and Systems** 

End Semester Exam

Date: 29th Nov. 2011 Time: 180 Minutes Max Marks. 80

Notes: All questions are compulsory.

Marks of each question are mention against it.

Assumptions made should be written clearly.

**1:** You are provided with a block **MinMax2** with 2 inputs – A and B, and 2 outputs – Max and Min. If we connect the 2 n-bit numbers at the inputs and the component drives the Max output with the bigger of the two and the Min output with the smaller of the two. Design a component – **MinMax4**, with 4 inputs and 4 outputs which sorts the 4 numbers using only **MinMax2** components. **[10]**

**2:** Derive the state diagram for an FSM that has the input w and output z. The machine has to generate output z = 1 when the previous 4 values of w are 1001 or 1111; otherwise z= 0. **[10]**

**3:** Design a counter that counts the pulses on line w and displays the count in the sequence 0, 2, 1, 3, 0, 2 …. Use D flip-flops in your circuit. **[7]**

**4:** You are provided with a 50 kHz square wave “x” with 5 Volts magnitude. X is connected as input to a block **BLACKBOX** which has one speaker at output end. Design the circuit for the block using JK flip flops such that once the circuit is switched on, speaker produces a sound. **[5]**

**5:** Given a 7 bit vector **x**, design a system that counts the number of 1’s in the vector using only Full Adders. **[8]**

*Hint: Don’t try to use K-maps or QM methods and save your time.*

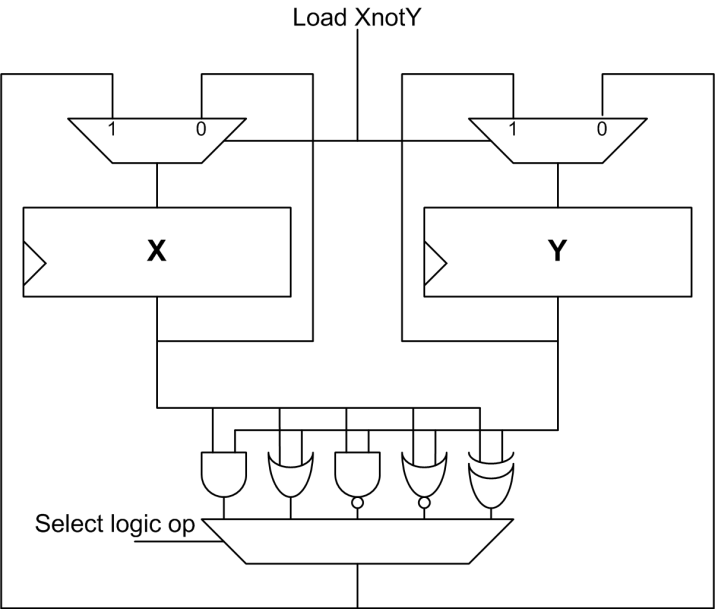
**6:** Using a module-16 binary counter with parallel inputs, implement a counter that counts the following periodic sequence: 0, 1, 2, 3, 4, 5, 8, 9, 10, 11, 14, 15. **[10]**

**7:** Implement the function F = (A nand B) or (B nand C) or (C nor D) using a 3 stage alternate nMOS-pMOS cascade logic. **[7]**

**8:** Analyze the circuit given in Figure 1 and derive the state table. **[8]**

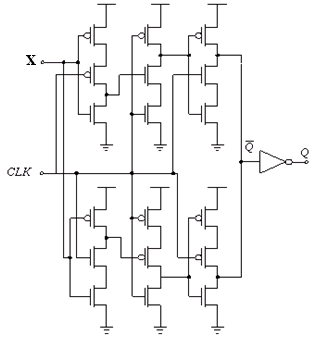
**Figure 2**

**9:** In the diagram given in figure 2 both X and Y are n-bit wide registers. With each clock cycle you could select a bit-wise basic operation between X and Y and load it to either X or Y, while the other register keeps its value. You have to exchange the contents of X and Y. Describe the values of the “**select logic op**” and “**load XnotY**” signals for each clock cycle. **[10]**

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**Figure 2:**

**10:** Analyze the figure 3 and derive the truth table as well as function implemented. **[5]**

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**Figure 3:**